

## CLAIMS

What is Claimed is:

1. A semiconductor device having a surface, comprising:

a plurality of conductive sub-surface regions of a first conductivity each formed

5 beneath said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter;

an isolation structure formed within said perimeter of said sub-surface structure such that said isolation structure creates a gap in said sub-surface structure; and

10 at least one metal structure formed above said surface, wherein said metal structure spans said gap and is coupled to said sub-surface structure via a plurality of tap contacts.

2. The semiconductor device as recited in Claim 1 wherein said sub-

15 surface structure is a diagonal sub-surface mesh structure.

3. The semiconductor device as recited in Claim 1 wherein said sub-surface structure is an axial sub-surface mesh structure.

20 4. The semiconductor device as recited in Claim 1 wherein said sub-surface structure is a diagonal sub-surface strip structure.

5. The semiconductor device as recited in Claim 1 wherein said sub-surface structure is an axial sub-surface strip structure.

6. The semiconductor device as recited in Claim 1 wherein each conductive  
5 sub-surface region has an N-type doping.

7. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a P-type doping.

10 8. The semiconductor device as recited in Claim 1 wherein each conductive sub-surface region has a strip shape.

9. The semiconductor device as recited in Claim 1 wherein said metal structure has a metal wire shape.

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10. The semiconductor device as recited in Claim 1 further comprising a plurality of second conductive sub-surface regions of said first conductivity each formed under each portion of said metal structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

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11. A semiconductor device having a surface, comprising:

a first plurality of conductive sub-surface regions of a first conductivity each formed beneath said surface, wherein said first plurality of conductive sub-surface regions form a first sub-surface structure for routing a body-bias voltage;

5 a second plurality of conductive sub-surface regions of said first conductivity each formed beneath said surface, wherein said second plurality of conductive sub-surface regions form a second sub-surface structure for routing said body-bias voltage;

an isolation structure formed between said first sub-surface structure and said second sub-surface structure such that said isolation structure creates a gap between said first sub-surface structure and said second sub-surface structure; and

10 at least one metal structure formed above said surface, wherein said metal structure spans said gap and is coupled to said first sub-surface structure and said second sub-surface structure via a plurality of tap contacts.

12. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first diagonal sub-surface mesh structure, and wherein said  
15 second sub-surface structure is a second diagonal sub-surface mesh structure.

13. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first axial sub-surface mesh structure, and wherein said second  
20 sub-surface structure is a second axial sub-surface mesh structure.

14. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first diagonal sub-surface strip structure, and wherein said second sub-surface structure is a second diagonal sub-surface strip structure.

5 15. The semiconductor device as recited in Claim 11 wherein said first sub-surface structure is a first axial sub-surface strip structure, and wherein said second sub-surface structure is a second axial sub-surface strip structure.

10 16. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has an N-type doping.

17. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has a P-type doping.

15 18. The semiconductor device as recited in Claim 11 wherein each conductive sub-surface region has a strip shape.

19. The semiconductor device as recited in Claim 11 wherein said metal structure has a metal wire shape.

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20. The semiconductor device as recited in Claim 11 further comprising a plurality of second conductive sub-surface regions of said first conductivity each formed under each portion of said metal structure that overlaps said first and second

sub-surface structures, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

21. A semiconductor device having a surface, comprising:

5 a plurality of conductive sub-surface regions of a first conductivity each formed beneath said surface, wherein said conductive sub-surface regions form a sub-surface structure for routing a body-bias voltage, wherein said sub-surface structure has a perimeter;

an isolation structure formed within said perimeter of said sub-surface structure  
10 such that said isolation structure creates a gap in said sub-surface structure; and  
at least one structure that spans said gap and is coupled to said sub-surface structure.

22. The semiconductor device as recited in Claim 21 wherein said sub-  
15 surface structure is a diagonal sub-surface mesh structure.

23. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is an axial sub-surface mesh structure.

20 24. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is a diagonal sub-surface strip structure.

25. The semiconductor device as recited in Claim 21 wherein said sub-surface structure is an axial sub-surface strip structure.

26. The semiconductor device as recited in Claim 21 wherein each  
5 conductive sub-surface region has an N-type doping.

27. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a P-type doping.

10 28. The semiconductor device as recited in Claim 21 wherein each conductive sub-surface region has a strip shape.

29. The semiconductor device as recited in Claim 21 wherein said structure is a polysilicon wire.

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30. The semiconductor device as recited in Claim 21 wherein said structure is a diffusion wire.

31. The semiconductor device as recited in Claim 21 wherein said structure  
20 is a silicide wire.

32. The semiconductor device as recited in Claim 21 further comprising a plurality of second conductive sub-surface regions of said first conductivity each

formed under each portion of said structure that overlaps said sub-surface structure, wherein each second conductive sub-surface region has a continuous sub-surface layer shape.

- 5            33.    The semiconductor device as recited in Claim 21 wherein said isolation structure divides said sub-surface structure into a first portion and a second portion.